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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,401	KIM, DU-YEUL	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-16* is/are rejected.

7)☒ Claim(s) *4-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed July 20, 2006 in response to the Office action dated April 21, 2006. Claims 3, 15, and 16 have been amended. Claims 1-16 are pending in this application.

OBJECTIONS

Drawings

1. In view of Applicant's amendment, the objections to the drawings have been withdrawn.

Specification

2. In view of Applicant's amendment, the previous objections to the specification have been withdrawn.

3. **Claim 3** is objected to because of the following informalities: On 3, the word "compromises" should read "comprises."

Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

4. In view of Applicant's amendment, the 112, 1st paragraph rejections to **claims 2-3 and 15** have been withdrawn.

5. In view of Applicant's amendment, the 112, 2nd paragraph rejections to **claims 3 and 10-13** have been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 and 6-14 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's "Description of the Related Art" appearing in Applicant's specification and drawings, hereafter referred to as "Applicant's admitted prior art" in view of Lee (U.S. Patent 6,564,287).

8. **As per claim 1**, Applicant's admitted prior art discloses a pipeline memory device comprising:

a plurality of memory cells that store data (paragraph 0004, lines 3-5; Fig. 1, elements 21 and 22);

a data transfer path on which the data is transferred (paragraph 0005, lines 6-9; Fig. 1, element 32); *It should be noted that "data pipeline stage" is analogous to "data transfer path."*

a first pipeline stage which latches the data on the data transfer path in response to the first pipeline control signal (paragraph 0005, lines 9-13; Fig. 1, element 26);

a second pipeline stage which latches the data latched by the first pipeline stage in response to the second pipeline control signal (paragraph 0005, lines 9-13; Fig. 1, element 28);

and a third pipeline stage which outputs the data latched by the second pipeline stage to a data output pad in response to a data output clock signal (paragraph 0005, lines 9-13; Fig. 1, elements 30 and 34). *It should be noted that "data output buffer" is analogous to "data output pad."*

Applicant's prior art does not expressly disclose a data fetching control circuit which generates:

a first pipeline control signal, in response to a first clock signal for generating the first pipeline control signal;

and a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal.

Lee discloses a data fetching control circuit which generates:

a first pipeline control signal, in response to a first clock signal for generating the first pipeline control signal (col. 3, lines 22-28; Fig. 3, elements p3 and CLK); *It should be noted that "pipeline control signal p3" is analogous to "first pipeline control signal" and "clock signal CLK" is analogous to "first clock signal."*

and a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal (col. 3, lines 34-37; Fig. 3, elements 56, p2, and p3). *It should be noted that "pipeline control signal p2" is analogous to "second pipeline control signal." It should also be noted that*

*p3 is **both** a control signal **and** a clock signal. p3 is merely a buffered version of "clock signal CLK." p3 also acts as a control signal which is sent to from the "pipeline control signal generation circuit" to the "pipeline circuit" (Fig. 1, elements 28 and 30). Therefore, p3 is analogous to **both** a "second clock signal" **and** a "first pipeline control signal." Since p2 is created in response to p3 it follows that Lee discloses "a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal."*

Applicant's admitted prior art and Lee are analogous art because they are from the same field of endeavor, that being pipeline memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Lee's pipeline control signal generation circuit and implement the generated pipeline control signals p3 and p2 within Applicant's admitted prior art's first and second stages of the pipeline memory device.

The motivation for doing so would have been to provide variable operation modes of latency and variable operation modes of burst length, thus increasing system flexibility and improving performance.

Therefore, it would have been obvious to combine Applicant's admitted prior art and Lee for the benefit of obtaining the invention as specified in claim 1.

9. **As per claim 6**, Applicant's admitted prior art discloses a data fetching method for a pipeline memory device, comprising:

transferring data stored in memory cells along a transfer path (paragraph 0005, lines 6-9; Fig. 1, element 32);

latching the data to a first pipeline stage on the transfer path in response to the first pipeline control signal (paragraph 0005, lines 9-13; Fig. 1, element 26);

latching the data to a second pipeline stage on the transfer path in response to the second pipeline control signal (paragraph 0005, lines 9-13; Fig. 1, element 28);

and outputting the data from the second pipeline stage to a data output pad in response to a data output clock signal (paragraph 0005, lines 9-13; Fig. 1, elements 30 and 34). *Please see citation notes for similar limitations in claim 1 above.*

Applicant's admitted prior art does not expressly disclose generating a first pipeline control signal in response to a first clock signal for generating a first pipeline control signal;

generating a second pipeline control signal in response to a second clock signal for generating a second pipeline control signal and the first pipeline control signal.

Lee discloses generating a first pipeline control signal in response to a first clock signal for generating a first pipeline control signal (col. 3, lines 22-28; Fig. 3, elements p3 and CLK);

generating a second pipeline control signal in response to a second clock signal for generating a second pipeline control signal and the first pipeline control signal (col. 3, lines 34-37; Fig. 3, elements 56, p2, and p3). *Please see citation notes for similar limitations in claim 1 above.*

Applicant's admitted prior art and Lee are analogous art because they are from the same field of endeavor, that being pipeline memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Lee's pipeline control signal generation circuit and implement the generated pipeline control signals p3 and p2 within Applicant's admitted prior art's first and second stages of the pipeline memory device.

The motivation for doing so would have been to provide variable operation modes of latency and variable operation modes of burst length, thus increasing system flexibility and improving performance.

Therefore, it would have been obvious to combine Applicant's admitted prior art and Lee for the benefit of obtaining the invention as specified in claim 6.

10. **As per claim 7**, the combination of Applicant's admitted prior art/Lee discloses a point of activation of the second pipeline control signal is determined depending on a point of activation of the first pipeline control signal (Lee, col. 3, lines 34-37; Fig. 6, time diagrams for p3 and p2). *It should be noted that since p2 directly dependent on p3 it is inherently required p2 is activated at some point after p3 has been activated. The time diagrams from Fig. 6 confirm that p2 is activated after p3 has been activated.*

11. **As per claim 8**, the combination of Applicant's admitted prior art/Lee discloses the second pipeline control signal is activated when the first pipeline control signal is inactive (Lee, Fig. 6, time diagrams for p3 and p2). *It should be noted that when looking at Fig. 6 it is clear that p2 goes high (active) for the first time after p3 goes low (inactive) for the first time.*

12. **As per claim 9**, Applicant's admitted prior art discloses an apparatus comprising:

at least one memory cell (paragraph 0004, lines 3-5; Fig. 1, element 21);

a first pipeline stage coupled to the output of the at least one memory cell, wherein the first pipeline stage is driven by a first control signal (paragraph 0005; Fig. 1, elements 21, 24, and 26);

and a second pipeline stage coupled to the output of the first pipeline stage, wherein the second pipeline stage is driven by a second control signal (paragraph 0005, lines 9-13; Fig. 1, elements 26-28).

Applicant's admitted prior art does not expressly disclose the second pipeline stage is driven by the first control signal and a second control signal.

Lee discloses a second control signal driven by a first control signal (col. 3, lines 34-37; Fig. 3, elements 56, p2, and p3).

Applicant's admitted prior art and Lee are analogous art because they are from the same field of endeavor, that being pipeline memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Lee's pipeline control signal generation circuit and implement the generated pipeline control signals p3 and p2 within Applicant's admitted prior art's first second stage of the pipeline memory device.

The motivation for doing so would have been to provide variable operation modes of latency and variable operation modes of burst length, thus increasing system flexibility and improving performance.

Therefore, it would have been obvious to combine Applicant's admitted prior art and Lee for the benefit of obtaining the invention as specified in claim 9.

13. **As per claim 10**, the combination of Applicant's admitted prior art/Lee discloses the first control signal and the second control signal are driven by a clock signal (Lee, col. 3, lines 22-28 and 34-37; Fig. 3, elements p3, p2, and CLK). *It should be noted that CLK drives p3 and p3 in turn drives p2, therefore, CLK inherently drives both p3 and p2.*

14. **As per claim 11**, the combination of Applicant's admitted prior art/Lee discloses the clock signal is an internal clock signal (Lee, col. 3, lines 25). *It should be noted that "CLK" is analogous to "PCLK."*

15. **As per claim 12**, the combination of Applicant's admitted prior art/Lee discloses the first control signal is delayed from the clock signal by a first delay (Lee, Fig. 6, time diagrams for p3 and CLK); *It should be noted that the "first delay" between CLK and p3 is taken from a falling edge of CLK until the next full rising edge of p3.*

and the second control signal is delayed from the clock signal by a second delay (Lee, Fig. 6, time diagrams for p2 and CLK). *It should be noted that the "second delay" between CLK and p2 is taken from a falling edge of CLK until the next full rising edge of p2.*

16. **As per claim 13**, the combination of Applicant's admitted prior art/Lee discloses the first delay is larger than the second delay (Lee, Fig. 6, time diagrams for p3, p2, and CLK). *It should be noted that time (i.e. delay) from a falling edge of CLK until the next full rising edge of p3 is larger than the time from a falling edge of CLK until the next full rising edge of p2.*

17. **As per claim 14**, the combination of Applicant's admitted prior art/Lee discloses the first control signal and the second control signal are never in an active state at the

same time (Lee, Fig. 6, time diagrams for p3 and p2). *It should be noted that p3 is only high (active) when p2 is low (inactive) and vice versa.*

18. Claims 2-3 and 15 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Lee as applied to claims 1 and 9 above, and in further view of Paul et al. (U.S. Patent 6,629,226).

19. **As per claim 2**, Applicant's admitted prior art/Lee discloses a first edge trigger delay circuit which receives the first clock signal for generating the first pipeline control signal and generates the first pipeline control signal (Applicant's admitted prior art, paragraph 0009, lines 1-5); *It should be noted that "internal clock signal PCLK" is analogous to "first clock signal."*

Applicant's admitted prior art/Lee does not expressly disclose a multiplexer which receives the second clock signal for generating the second pipeline control signal and the first pipeline control signal, and generates the second pipeline control signal.

Paul discloses a multiplexer which receives the second clock signal for generating the second pipeline control signal and the first pipeline control signal, and generates the second pipeline control signal (col. 5, lines 45-51; Fig. 5, elements 164, 165, ADDRESS (@SYSCLK), and CTR). *It should be noted that "ADDRESS (@SYSCLK)" is analogous to "second clock signal" and "CTR" is analogous to "first pipeline control signal." It should also be noted that the output of "MUX 164" is analogous to the "second pipeline control signal."*

Applicant's admitted prior art/Lee and Paul are analogous art because they are from the same field of endeavor, that being pipeline memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Paul's MUX which uses a control signal and clock signal to create another control signal to drive a pipeline stage within Applicant's admitted prior art/Lee's the pipeline memory device.

The motivation for doing so would have been to eliminate synchronizing problems with configuration dependent latencies (Paul, col. 2, lines 45-46).

Therefore, it would have been obvious to combine Applicant's admitted prior art/Lee and Paul for the benefit of obtaining the invention as specified in claim 2.

20. **As per claim 3**, the combination of Applicant's admitted prior art/Lee/Paul discloses the first edge trigger delay circuit compromises an even number of inverters in a chain (Applicant's admitted prior art, paragraph 0009, line 1; Fig. 3, element 300).

21. **As per claim 15**, the combination of Applicant's admitted prior art/Lee/Paul discloses the second pipeline stage is driven by the first control signal, and the second control signal utilizes a multiplexer (Paul, col. 5, lines 48-51; Fig. 5, elements 164, 165, and CTR). *Please see citation notes for claim 2 above.*

22. Claim 16 is rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Lee as applied to claim 9 above, and in further view of Shinozaki (U.S. Patent 6,084,802).

23. Applicant's admitted prior art/Lee discloses all the limitations of claim 16 except the second pipeline stage is driven by the first control signal, and the second control signal utilizes a NAND gate.

Shinozaki discloses the second pipeline stage is driven by the first control signal, and the second control signal utilizes a NAND gate (col. 8, lines 42-47; Fig. 8, elements 42, 43, and Hz). *It should be noted that "Hz" is analogous to "first control signal" and "drive signal 42" is analogous to "second control signal."*

Applicant's admitted prior art/Lee and Shinozaki are analogous art because they are from the same field of endeavor, that being pipeline memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Shinozaki's NAND gate with two control signals used to drive the second stage of the pipe-line circuit within Applicant's admitted prior art/Lee's second stages of the pipeline memory device.

The motivation for doing so would have been to provide a semiconductor memory device which can keep the timing of an output signal from an output circuit at a predetermined phase difference to a supplied external clock in accordance with the period of the external clock, and can guarantee the proper operation of internal circuits with a pipe-line structure (Shinozaki, col. 2, lines 3-9).

Therefore, it would have been obvious to combine Applicant's admitted prior art/Lee and Shinozaki for the benefit of obtaining the invention as specified in claim 16.

Response to Arguments

24. Applicant's arguments filed in the communication dated July 20, 2006 with respect to **claims 1-3 and 6-16** have been fully considered but they are not persuasive.

25. With respect to Applicant's arguments that start in the second full paragraph of page 11 through the first full paragraph of page 12 of the communication filed July 20, 2006, the Examiner respectfully disagrees. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicant is reminded that the Examiner has relied **only** upon the teaching of generating pipeline control signals in the manner disclosed by the pipeline control signal generation circuit in Fig. 3 of Lee in combination with Applicant's three pipeline stages disclosed as admitted prior art. Applicant alleges that "in order for the Office Action's construction to be correct, pipeline stage 64 would need to feed data to pipeline stage 62", however, this allegation is in error because the Examiner has never relied upon the three stage pipeline circuit disclosed in Fig. 4 of Lee. Thus, when individually taking the pipeline control signal generation circuit in Fig. 3 of Lee (and **not** the three stage pipeline circuit disclosed in Fig. 4 of Lee) and combining it with Applicant's three stage pipeline circuit disclosed as admitted prior art and, the pipeline control signal p3 from Lee can be fed into the first pipeline stage of Applicant's admitted prior art, therefore making p3 analogous to a first pipeline control signal.

26. With respect to Applicant's argument in the last full paragraph of page 12 through the second full paragraph of page 13 of the communication filed July 20, 2006, the Examiner respectfully disagrees. Applicant alleges that the Examiner's provided

motivation assertion is "problematic for a number of reasons." Applicant states that "First, the assertion does not appear in any of the cited art of record." The Examiner reminds Applicant, as stated in MPEP § 2143.01 (I), motivation to combine references need not be explicitly taught in the references because the Examiner's motivation assertion was knowledge generally available to one of ordinary skill in the art at the time of the invention. However, assuming arguendo, the Examiner cites as evidence Adkisson (U.S. Patent 5,590,304) to show that the Examiner's motivation assertion was knowledge generally available to one of ordinary skill in the art. Adkisson states "the burst length and burst frequency are programmable providing operational flexibility (col. 6, lines 3-5). Applicant also states "Second, by using clock signal p3 (as suggested by the Office Action) to control a first pipeline stage in the memory device of the DRA, there is no indication that the modified memory device would even be operable, much less exhibit improved performance and flexibility." Again, the Examiner reminds Applicant, as stated in MPEP § 2143.02, obviousness only requires a reasonable expectation of success. To this degree the Examiner asserts that feeding an output of Lee's pipeline control signal generation circuit into a stage of Applicant's admitted prior art's pipeline memory device would constitute a reasonable expectations of success.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

Allowable Subject Matter

27. **Claims 4 and 5** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

28. As allowable subject matter has been indicated, Applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

Claims Rejected in the Application

29. Per the instant office action, **claims 1-3 and 6-16** have received a second action on the merits and are subject of a second action final.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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September 21, 2006

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